

FIG. 1

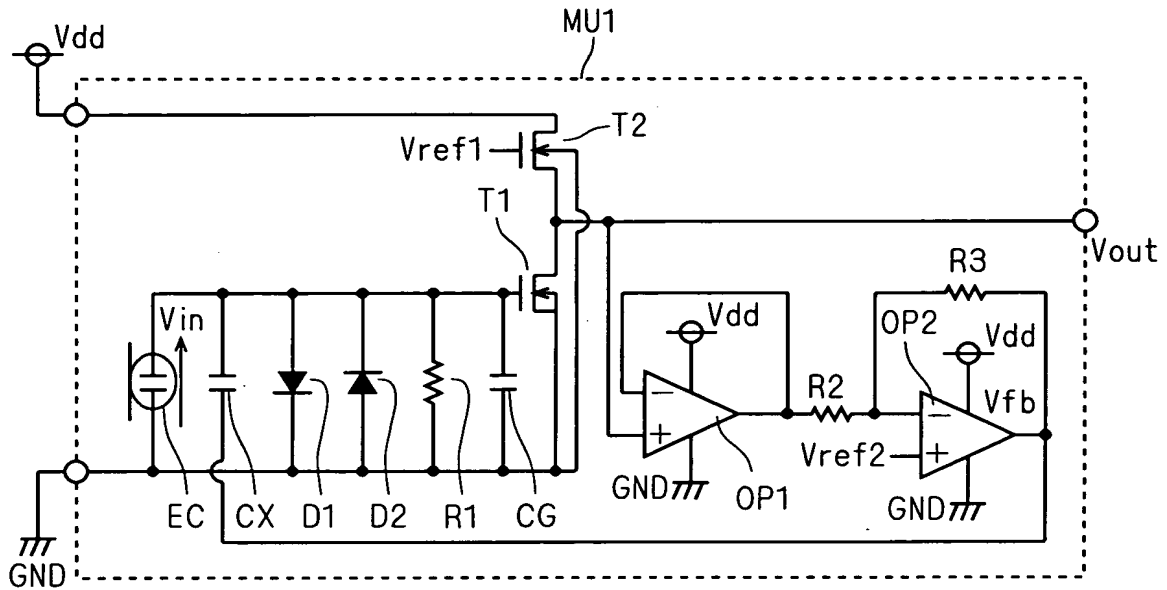


FIG. 2

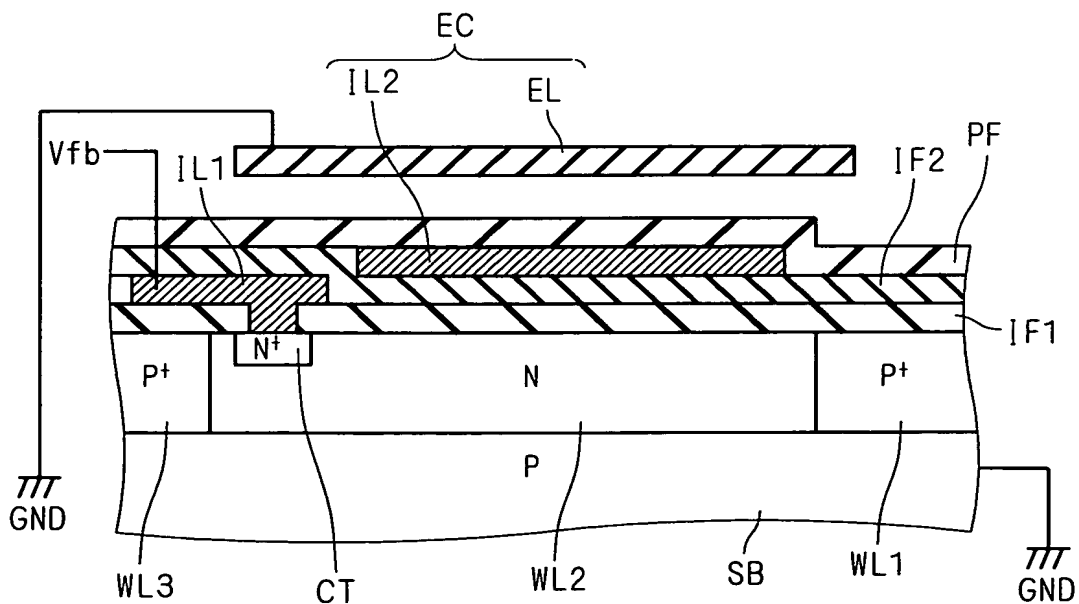


Diagram illustrating a cross-sectional view of a semiconductor device. The structure shows a substrate with layers P, N, and P+. A gate stack is formed on the substrate, consisting of layers IL1, IL3, and EL. A source/drain region is labeled N+. A contact layer CT is shown. The device is connected to a Vfb terminal and a GND terminal. Labels include WL3, WL2, WL1, SB, and PF.

FIG. 5

< BACKGROUND ART >

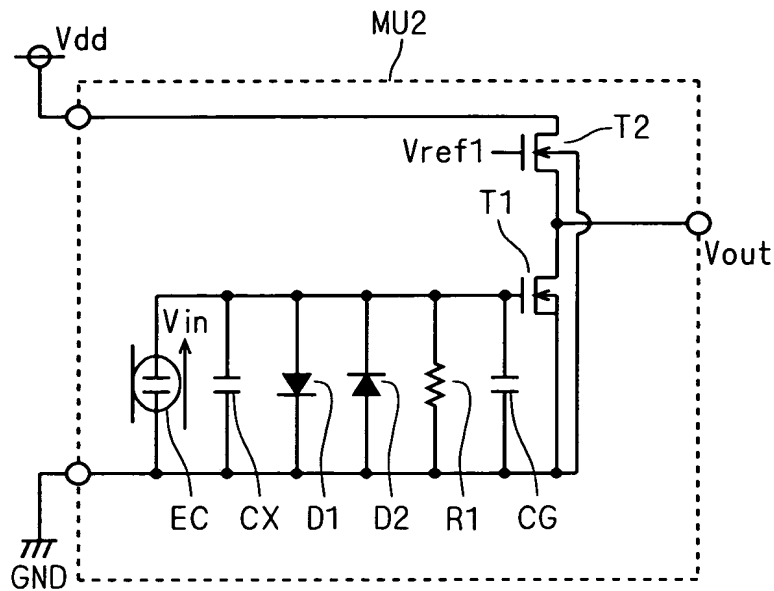


FIG. 6

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